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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,792	08/29/2001	Paul A. Farrar	M4065.0382/P382-A	5268
24998	7590	01/07/2005	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			LEE, EUGENE	
2101 L Street, NW			ART UNIT	
Washington, DC 20037			PAPER NUMBER	
			2815	
DATE MAILED: 01/07/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/940,792

Applicant(s)

FARRAR ET AL.

Examiner

Eugene Lee

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 46-48, 51-56, 58-60, 62-65 and 67-81 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 46-48, 51-56, 58-60, 62-65, 67-81 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 56, 58, 59, 72, and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. 5,963,838 in view of Yamagata et al. 5,679,475. Yamamoto discloses (see, for example, FIG. 47) a semiconductor device (buried conductor pattern) comprising a substrate 21, and wiring layer (conductive material) 32. The wiring layer fills an empty-spaced pattern having a plate/pipe-shaped pattern and forms a conductive path that extends to the surface of the substrate 21. A portion of the top surface of said wiring layer is below a top surface of said substrate and a portion of a bottom surface of said wiring layer is above a bottom surface of said substrate. The wiring layer is part of an interconnect between MOS transistors (devices) 34a. Yamamoto does not disclose a monocrystalline substrate. However, Yamagata discloses (see, for example, column 1, lines 51-53) that monocrystalline substrates have good controllability of crystal orientations and less crystal defects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a monocrystalline substrate in order to have good controllability of crystal orientations and less crystal defects.

Regarding the new limitation ("a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate") in claim 56, Yamamoto discloses a

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conductive layer (conductive path) 37 that connects the wiring layer 32 to the outside of substrate 21.

3. Claims 46, 51, 52, 54, 55, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. '838 in view of Yamagata et al. '475 as applied to claims 56, 58, 59, 72, and 75 above, and further in view of Sato et al. "A New Substrate Engineering for the Formation of Empty Space in Silicon Induced by Silicon Surface Migration." Yamamoto in view of Yamagata does not disclose a spherical pattern. However, Sato discloses (see, for example, column 2, lines 4-7) a spherical pattern as one of many patterns that are formed within a substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a spherical pattern in order to form a buried pattern that supports semiconductor devices under the surface of a substrate. Also the use of a spherical pattern does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

Regarding claim 51, see column 22, lines 13-15 wherein Yamamoto discloses the wiring layer being made of tungsten.

Regarding claim 52, see column 19, lines 30-35 wherein Yamamoto discloses a silicon substrate.

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4. Claims 47, 48, and 76 thru 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. '838 in view of Yamagata et al. '475 in view of Sato et al. "A New Substrate Engineering for the Formation of Empty Space in Silicon Induced by Silicon Surface Migration" as applied to claims 46, 51, 52, 54, 55, and 60 above, and further in view of Kenney 5,583,368. Yamamoto in view of Yamagata in view of Sato does not disclose a second buried conductor pattern having a pipe-shaped or plate-shaped pattern, and said first buried conductor pattern being located below said second buried conductor pattern. However, Kenney discloses (see, for example, FIG. 1g) subsurface structures (for contacts to and connectors between devices) comprising trenches of varying depths. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second buried conductor pattern having a pipe-shaped or plate-shaped pattern, and said first buried conductor pattern being located below said second buried conductor pattern in order to form multiple contacts within a semiconductor device and form greater circuit integration. In addition, the use of a spherical pattern with a plate-shaped or pipe-shaped pattern or any other combination of patterns within the same device does not provide any critical or unexpected results to the applicant's invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

5. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. '838 in view of Yamagata et al. '475 in view of Sato et al. "A New Substrate Engineering for the

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Formation of Empty Space in Silicon Induced by Silicon Surface Migration” as applied to claims 46, 51, 52, 54, 55, and 60 above, and further in view of Witek et al. 5,291,438. Yamamoto in view of Yamagata in view of Sato does not disclose said monocrystalline substrate being a germanium substrate. However, germanium is one of many conventional materials used in the fabrication of semiconductor devices. In column 3, lines 63-65, Witek discloses germanium as a substrate material. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a germanium substrate in order to support a semiconductor device on a substrate. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

6. Claims 62 thru 64, and 67 thru 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. ‘838 in view of Yamagata et al. ‘475 as applied to claims 56, 58, 59, 72, and 75 above, and further in view of Tsu et al. 6,294,420 B1. Yamamoto in view of Yamagata does not disclose a processor system and a circuit coupled to said processor comprising a conductive structure. However, Tsu discloses (see, for example, FIG. 4C and FIG. 6) a memory array comprising a processor coupled to additional circuitry. In column 8, lines 61-*, Tsu states that the memory array may be embedded into a larger integrated circuit device wherein the memory array is included with control circuitry on the same integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the semiconductor device of Yamamoto in view of Yamagata into a memory array like Tsu in order to utilize the device in memory circuits.

Regarding the new limitation (“a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate”) in claim 62, Yamamoto discloses a conductive layer (conductive path) 37 that connects the wiring layer 32 to the top surface of substrate 21.

7. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. ‘838 in view of Tsu et al. ‘420 B1 as applied to claims 62-64, and 67-71 above, and further in view of Sato et al. “A New Substrate Engineering for the Formation of Empty Space in Silicon Induced by Silicon Surface Migration.” Yamamoto in view of Tsu does not disclose a spherical pattern. However, Sato discloses (see, for example, column 2, lines 4-7) a spherical pattern as one of many patterns that are formed within a substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a spherical pattern in order to form a buried pattern that supports semiconductor devices under the surface of a substrate. Also the use of a spherical pattern does not provide any critical or unexpected results to the applicant’s invention. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, “Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

8. Claims 73 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. ‘838 in view of Yamagata et al. ‘475 in view of Sato et al. “A New Substrate Engineering for the Formation of Empty Space in Silicon Induced by Silicon Surface Migration”

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as applied to claims 46, 51, 52, 54, 55, and 60 above, and further in view of Kenney 5,583,368.

Yamamoto in view of Yamagata in view of Sato does not disclose a second buried conductor pattern having a pipe-shaped pattern. However, Kenney discloses (see, for example, FIG. 1g) subsurface structures (for contacts to and connectors between devices) comprising trenches (with a pipe-shaped pattern) of varying depths. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second buried conductor pattern having a pipe-shaped pattern in order to form multiple contacts within a semiconductor device and form a more intricate device.

Response to Arguments

9. Applicant's arguments filed 10/21/04 have been fully considered but they are not persuasive.

Regarding the applicant's argument on page 3 of the amendment filed 10/21/04 that the subject matter of claims 56, 58, 59, 72, and 75 would not have been obvious over Yamamoto in view of Yamagata, whether considered alone or in combination, this argument is not persuasive. Yamagata discloses (see, for example, column 1, lines 51-53) a monocrystalline silicon substrate and discloses the monocrystalline substrate having good controllability of crystal orientation and very less crystal defects. Clearly, it would have been obvious to one of ordinary skill in the art to modify Yamamoto by having a monocrystalline substrate in order to have good controllability of crystal orientation and very less crystal defects. Whether Yamagata discloses a "buried conductor pattern being completely surrounded by a monocrystalline material" like Yamamoto is not relevant since Yamagata clearly discloses that a monocrystalline substrate has good

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controllability of crystal orientation and very less crystal defects, characteristics that indisputably would be beneficial to any substrate in a semiconductor device.

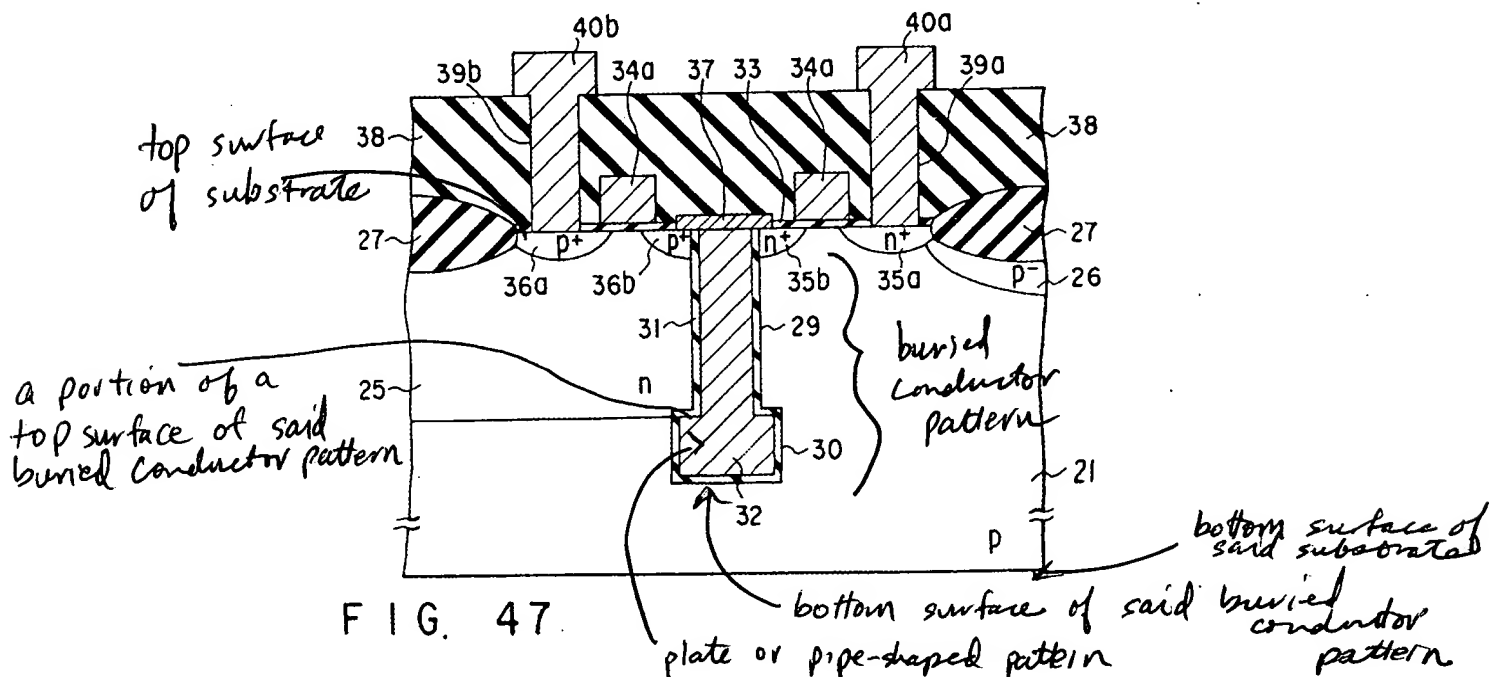
Regarding applicant's argument on page 4, that Yamamoto does not teach a "buried conductor pattern within a monocrystalline substrate", much less a "buried conductor pattern within a monocrystalline substrate" comprising "at least one empty-spaced pattern in said monocrystalline substrate formed by annealing said substrate containing at least one hole drilled therein, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration" as independent claim 56 recites, this argument is not persuasive. In FIG. 47, Yamamoto discloses a wiring layer (buried conductor pattern) 32 formed in a substrate 21 and the combination of Yamagata has already been disclosed as obvious as providing a monocrystalline substrate for good controllability of crystal orientation and very less crystal defects.

Regarding applicant's argument on page 4, end of the first paragraph that Yamamoto does not disclose, teach or suggest "a conductive path connecting said buried conductor pattern with the exterior of said monocrystalline substrate," as recited in independent claim 56, this argument is not persuasive. Yamamoto discloses a conductive layer (conductive path) 37 that connects the wiring layer (buried conductor pattern) 32 to the outside of substrate 21.

Regarding the applicant's argument on page 4, last paragraph that Yamamoto does not disclose, teach or suggest a "buried conductor pattern... being completely surrounded by monocrystalline material," this argument is not persuasive. In Yamamoto, wiring layer (buried conductor pattern) is completely surrounded by substrate 21, and the combination with Yamagata makes obvious that the substrate is monocrystalline.

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Regarding applicant's argument on page 5, first paragraph that Yamamoto is silent about "at least one buried conductor pattern provided within a monocrystalline substrate such that at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate" and further "having a plate-shaped pattern" or "having a pipe-shaped pattern", this argument is not persuasive. See FIG. 47 from Yamamoto below.



Regarding the applicant's argument on page 9 that a person of ordinary skill in the art would not have been motivated to combine the teaching of Yamamoto with those of Sato, this argument is not persuasive. Sato is simply used to show that the patterns in a substrate can be spherical shaped as well as pipe and plate shaped. The applicant's argument on page 10 that the empty space technique of Sato in lieu of the impurity implanting technique of Yamamoto would require a substantial reconstruction and redesign of the elements shown in Yamamoto is not

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persuasive since the claims are directed towards product, not method; and since the modification is simply varying the pattern of Yamamoto into a spherical pattern which Sato clearly discloses as one of many structural shapes that can be formed in a substrate.

Regarding applicant's argument on page 11 that Yamamoto, Yamagata, and Sato, whether considered alone or in combination, fail to teach as independent claim 76 recites, this argument is not persuasive. Claim 76 is unpatentable over Yamamoto in view of Yamagata in view of Sato in view of Kenney wherein Kenney discloses the first and second buried conductive patterns (as disclosed in the rejection above).

Regarding applicant's argument on page 13 that a person of ordinary skill in the art would not have been motivated to combine the teachings of Yamamoto with those of Tsu, this argument is not persuasive. Tsu discloses (see, for example, FIG. 6) a memory array comprising a processor coupled to additional circuitry and further states that the memory array may be embedded into a larger integrated circuit device wherein the memory array is included with control circuitry on the same integrated circuit. Therefore, it would have been obvious to include the device of Yamamoto in view of Yamagata into a memory array in order to implement the device into a more robust device such as a memory array.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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Eugene Lee

January 4, 2005


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2200